

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040208273 A1	20041021	11	CMOS lock detect with double protection	375/374
2	US 20030235260 A1	20031225	22	Methods and apparatus for generating timing signals	375/374
3	US 20030189991 A1	20031009	11	Charge pump phase locked loop	375/326
4	US 20030043949 A1	20030306	3353	Radio frequency data communications device	375/374
5	US 20030026372 A1	20030206	13	Adaptive phase locked loop	375/376
6	US 20020163986 A1	20021107	18	Method and apparatus for generating a phase dependent control signal	375/374
7	US 20020154721 A1	20021024	18	Method and apparatus for generating a phase dependent control signal	375/374
8	US 7054404 B2	20060530	38	Clock control method, frequency dividing circuit and PLL circuit	375/376
9	US 7016451 B2	20060321	17	Method and apparatus for generating a phase dependent control signal	375/374
10	US 7003066 B1	20060221	33	Digital phase locked loop with phase selector having minimized number of phase interpolators	375/376
11	US 6993108 B1	20060131	33	Digital phase locked loop with programmable digital filter	375/376
12	US 6977959 B2	20051220	20	Clock and data recovery phase-locked loop	375/219
13	US 6963629 B2	20051108	13	Adaptive phase locked loop	375/376
14	US 6952462 B2	20051004	19	Method and apparatus for generating a phase dependent control signal	375/373
15	US 6947513 B2	20050920	54	Radio frequency data communications device	375/374
16	US 6931086 B2	20050816	20	Method and apparatus for generating a phase dependent control signal	375/374

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1		Cao, Jun et al.
2		Nakamura, Katsufumi et al.
3	375/374	Puccio, Gianni et al.
4		O'Toole, James E. et al.
5	327/148; 327/157; 375/374; 375/375	Boerstler, David W. et al.
6	327/157	Harrison, Ronnie M.
7		Harrison, Ronnie M.
8	331/25; 375/374; 375/375	Saeki; Takanori
9		Harrison; Ronnie M.
10	375/374; 375/375	Davies; Antony et al.
11	375/374; 375/375	Chi; Kuang et al.
12	375/374; 375/375; 375/376	Brunn; Brian T. et al.
13	327/148; 327/157; 375/374; 375/375	Boerstler; David W. et al.
14	375/374	Harrison; Ronnie M.
15	340/10.1	O'Toole; James E. et al.
16	375/375	Harrison; Ronnie M.

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17	US 6853696 B1	20050208	26	Method and apparatus for clock recovery and data qualification	375/375
18	US 6819728 B2	20041116	32	Self-correcting multiphase clock recovery	375/376
19	US 6760394 B1	20040706	12	CMOS lock detect with double protection	375/374
20	US 6737995 B2	20040518	14	Clock and data recovery with a feedback loop to adjust the slice level of an input sampling circuit	341/68
21	US 6714772 B2	20040330	15	Wireless communication system	455/260
22	US 6590949 B1	20030708	7	Circuit and method for compensating a phase detector	375/376

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17	375/371; 375/372; 375/373; 375/374; 375/376	Moser; James et al.
18	327/148; 327/157; 370/518; 375/374	Boerstler; David William
19	327/156; 327/159; 331/25; 331/DIG.2 ; 375/376	Cao; Jun et al.
20	375/317; 375/374; 375/375; 375/376	Ng; Devin Kenji et al.
21	327/156; 327/157; 375/374; 375/375; 455/259; 455/262; 455/264	Kasahara; Masumi et al.
22	327/147; 327/148; 327/156; 327/157; 375/374	Marten; Lance Alan et al.

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23	US 6531927 B1	20030311	10	Method to make a phase-locked loop's jitter transfer function independent of data transition density	331/25
24	US 6526111 B1	20030225	10	Method and apparatus for phase locked loop having reduced jitter and/or frequency biasing	375/376
25	US 6526109 B1	20030225	30	Method and apparatus for hybrid smart center loop for clock data recovery	375/371
26	US 6470060 B1	20021022	15	Method and apparatus for generating a phase dependent control signal	375/374
27	US 6466634 B1	20021015	58	Radio frequency data communications device	375/374
28	US 6442225 B1	20020827	13	Multi-phase-locked loop for data recovery	375/376
29	US 6330296 B1	20011211	11	Delay-locked loop which includes a monitor to allow for proper alignment of signals	375/376
30	US 6314150 B1	20011106	9	Lock detector circuit for a phase-locked loop	375/374
31	US 6215834 B1	20010410	8	Dual bandwidth phase locked loop frequency lock detection system and method	375/375

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23	327/156; 327/157; 327/159; 331/1A; 331/14; 375/371; 375/373; 375/374; 375/375; 375/376; 713/400	Chen; Dao-Long
24	327/157; 375/374; 375/375	Prasad; Ammisetti V
25	327/158; 375/374; 375/376	Chang; Charles et al.
26	327/141; 327/142; 327/148; 327/157; 327/3; 375/373; 375/375	Harrison; Ronnie M.
27	340/10.1	O'Toole; James E. et al.
28	375/374	Huang; Chen-chih
29	327/159; 375/374	Atallah; Francois Ibrahim et al.
30	327/150; 327/151; 327/159; 331/DIG.2 ; 375/376	Vowe; Achim
31	331/14; 331/25; 375/362; 375/374	McCollough; Kelvin

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32	US 6157691 A	20001205	9	Fully integrated phase-locked loop with resistor-less loop filter	375/376
33	US 5987085 A	19991116	10	Clock recovery circuit	375/374
34	US 5978425 A	19991102	15	Hybrid phase-locked loop employing analog and digital loop filters	375/374
35	US 5945855 A	19990831	16	High speed phase lock loop having high precision charge pump with error cancellation	327/157
36	US 5910741 A	19990608	16	PLL circuit with non-volatile memory	327/150
37	US 5901184 A	19990504	15	Extended range voltage controlled oscillator for frequency synthesis in a satellite receiver	375/344
38	US 5889828 A	19990330	103	Clock reproduction circuit and elements used in the same	375/374

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32	327/148; 327/149; 327/150; 327/156; 375/373; 375/374	Wei; Shuran
33	327/157; 331/10; 331/25; 375/375; 375/376	Anderson; Michael B.
34	327/159; 331/10; 375/375; 375/376	Takla; Ashraf K.
35	327/156; 327/536; 327/537; 375/373; 375/374	Momtaz; Afshin D.
36	327/148; 327/157; 327/159; 331/1A; 331/16; 331/DIG.2 ; 331/DIG.3 ; 375/374	Watanabe; Hiroyuki
37	348/731; 348/733; 375/345; 375/371; 375/374; 725/68	Ben-Efraim; Nadav et al.
38	327/154; 375/375; 375/376	Miyashita; Takumi et al.

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39	US 5822387 A	19981013	11	Apparatus for fast phase-locked loop (PLL) frequency slewing during power on	375/376
40	US 5799048 A	19980825	12	Phase detector for clock synchronization and recovery	375/360
41	US 5740213 A	19980414	27	Differential charge pump based phase locked loop or delay locked loop	375/374
42	US 5610954 A	19970311	103	Clock reproduction circuit and elements used in the same	375/375
43	US 5566212 A	19961015	8	Phase-locked loop circuit for Manchester-data decoding	375/333
44	US 5481563 A	19960102	8	Jitter measurement using a statistically locked loop	375/226
45	US 5408200 A	19950418	10	Intelligent phase detector	331/1A
46	US 5349612 A	19940920	14	Digital serializer and time delay regulator	375/371
47	US 5276716 A	19940104	17	Bi-phase decoder phase-lock loop in CMOS	375/376
48	US 5245637 A	19930914	12	Phase and frequency adjustable digital phase lock logic system	375/374

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39	375/374; 375/375	Mar; Monte F.
40	327/144; 327/157; 327/159; 331/17; 375/374	Farjad-Rad; Ramin et al.
41	327/157; 331/17	Dreyer; Stephen F.
42	327/157; 331/25; 375/374	Miyashita; Takumi et al.
43	375/359; 375/361; 375/374; 375/376	Boytim; Mathew A. et al.
44	375/355; 375/359; 375/371; 375/374; 375/376	Hamre; John D.
45	327/156; 327/292; 331/11; 331/12; 331/25; 360/51; 375/371; 375/374; 375/376	Buhler; Otto
46	327/270; 375/374	Guo; Bin et al.
47	331/1A; 375/374; 375/375	Winen; John M.
48	327/141; 327/231	Gersbach; John E. et al.

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49	US 5239561 A	19930824	12	Phase error processor	375/376
50	US 5095498 A	19920310	19	Bit synchronizer	375/340
51	US 5081655 A	19920114	10	Digital phase aligner and method for its operation	375/373
52	US 5036528 A	19910730	12	Self-calibrating clock synchronization system	375/374
53	US 4890305 A	19891226	4	Dual-tracking phase-locked loop	375/374
54	US 4821296 A	19890411	18	Digital phase aligner with outrigger sampling	375/374
55	US 4780844 A	19881025	12	Data input circuit with digital phase locked loop	710/58
56	US 4700347 A	19871013	9	Digital phase adjustment	714/700
57	US 4633488 A	19861230	15	Phase-locked loop for MFM data recording	375/374
58	US 4590602 A	19860520	9	Wide range clock recovery circuit	375/375

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49	327/231; 329/307; 329/309; 329/310; 329/325; 331/1A; 331/25; 375/374	Wong; Hee et al.
50	327/141; 327/2; 375/362; 375/374	DeLuca; Michael J. et al.
51	327/231; 331/1A; 375/374	Long; John R.
52	327/231; 327/3; 331/18	Le; Duc N. et al.
53	331/1A; 375/327; 375/376	Devries; Paul A.
54	375/362	Cordell; Robert R.
55	360/51; 375/374; 713/502	Keller; Glenn
56	327/250; 327/284; 375/374	Rettberg; Randall D. et al.
57	327/157; 331/1A; 360/61; 375/359; 375/376	Shaw; Robert A.
58	331/1A; 331/DIG.2 ; 375/328; 375/374; 375/376	Wolaver; Dan H.

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59	US 4546486 A	19851008	10	Clock recovery arrangement	375/374
60	US 4534044 A	19850806	10	Diskette read data recovery system	375/374
61	US 4464771 A	19840807	8	Phase-locked loop circuit arrangement	375/374
62	US 4320527 A	19820316	11	Bit synchronizing system for pulse signal transmission	375/374
63	US 4280099 A	19810721	15	Digital timing recovery system	327/160
64	US 4216544 A	19800805	6	Digital clock recovery circuit	375/374
65	US 4029900 A	19770614	22	Digital synchronizing signal recovery circuits for a data receiver	375/365
66	US 3626306 A	19711207	8	AUTOMATIC BAUD SYNCHRONIZER	327/141

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59	327/5; 375/361; 375/376	Evans; Michael W.
60	331/1A; 360/51; 375/376	Funke; Michael J. et al.
61	327/157; 331/1A; 331/17; 375/376	Sorensen; Bendt H.
62	327/113; 327/141; 327/47	Takasaki; Yoshitaka
63	327/166; 327/299; 327/98; 375/374	Rattlingourd; Glen D.
64	327/166; 327/241; 377/43; 377/45; 377/50	Boleda; Alberto et al.
65	327/155; 375/374; 375/376	Addeo; Eric John
66	327/161; 341/56; 375/355; 375/373; 375/374	Puckette; Charles McD.